library ieee;

use ieee.std\_logic\_1164.all;

use ieee.std\_logic\_arith.all;

use ieee.std\_logic\_unsigned.all;

entity LIFO is

port(clk,reset,pop,push: in bit;

I: in bit\_vector(3 downto 0);

O: out bit\_vector(3 downto 0));

end LIFO;

architecture A of LIFO is

component LIFO\_cell is

port(reset,clk,SerialIn,pop,push: in bit;

dataOut: out bit);

end component;

begin

L1: LIFO\_CELL port map(reset,clk,I(3),pop,push,O(3));

L2: LIFO\_CELL port map(reset,clk,I(2),pop,push,O(2));

L3: LIFO\_CELL port map(reset,clk,I(1),pop,push,O(1));

L4: LIFO\_CELL port map(reset,clk,I(0),pop,push,O(0));

end A;

library ieee;

use ieee.std\_logic\_1164.all;

use ieee.std\_logic\_arith.all;

use ieee.std\_logic\_unsigned.all;

entity LIFO\_cell is

port(reset,clk,SerialIn,pop,push: in bit;

dataOut: out bit);

end LIFO\_cell;

architecture LIFO1 of LIFO\_cell is

begin

process(clk,reset,serialIn,pop,push)

variable state: bit\_vector(3 downto 0):="0000";

begin

if reset = '1' then

state := "0000";

elsif clk='1' and clk'event then

if pop=push then

state:=state;

else

if push = '1' then

state := state srl 1;

state(3):=serialIn;

end if;

if pop = '1' then

dataOut<=state(3);

end if;

end if;

end if;

end process;

end LIFO1;